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**To:** Examiner Sanh D. Phu / U.S. Patent & Trademark Office

**From:** Maximilian R. Petersson

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**Pages:** 13

**Phone:** (571) 272-7857

**Date:** October 5, 2005

**Re:** USSN 10/079,057 entitled, "Apparatus and Method for Front-End Circuitry in Radio-Frequency Apparatus"; Filed February 19, 2002

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● **Comments:**

Amendment and Interview Summary

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of: ERIC R. GARLEPP ET AL.

Filed: FEBRUARY 19, 2002

For: APPARATUS AND METHOD FOR FRONT-END CIRCUITRY IN  
RADIO-FREQUENCY APPARATUS

Serial No.: 10/079,057

Group Art Unit: 2682

Examiner: PHU, SANH D.

Atty Dkt: SILA:107

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being transmitted via facsimile to (571) 273-7857 and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below:

10/5/05  
Date

Karen Fowler  
Name

Commissioner for Patents  
P.O. Box 1450  
Alexandria 22313-1450

**AMENDMENT AND INTERVIEW SUMMARY**

Dear Sir:

The Applicant submits this paper in response to a telephone discussion with the Examiner on October 5, 2005 ("Interview").

## AMENDMENT

Please amend the application as follows:

### In the Claims:

Please amend the claims 1, 35, and 63 as follows. The following provides the claims and their status.

1. (currently amended) A front-end circuitry in a radio-frequency (RF) apparatus, comprising:  
  
a filter circuitry with a differential output, having an output impedance, the filter circuitry configured to filter signals outside a signal band of interest, the filter circuitry configured to receive and filter a radio-frequency (RF) signal; and  
  
an impedance matching network, with a differential input coupled to the output of the filter circuitry, the differential input having symmetrical impedances from input signal lines to a reference node, the impedance matching network further having a differential output coupled to a signal processing circuitry having an input impedance, the differential output having symmetrical impedances from output signal lines to the reference node,  
  
wherein the impedance matching network matches the input impedance of the signal processing circuitry to the output impedance of the filter circuitry.
- 2-3. (canceled).
4. (previously presented) The front-end circuitry according to claim 1, wherein the signal processing circuitry comprises an amplifier circuitry.
5. (previously presented) The front-end circuitry according to claim 4, wherein signal processing circuitry comprises a low-noise amplifier circuitry.
6. (previously presented) The front-end circuitry according to claim 5, wherein the impedance matching network comprises a differential L-network.

7. (previously presented) The front-end circuitry according to claim 6, wherein the signal processing circuitry comprises a single-ended output.
8. (previously presented) The front-end circuitry according to claim 6, wherein the signal processing circuitry comprises a differential output.
9. (previously presented) The front-end circuitry according to claim 6, wherein the differential L-network comprises two inductors and a capacitor.
10. (previously presented) The front-end circuitry according to claim 6, wherein the differential L-network comprises two capacitors and an inductor.
11. (previously presented) The front-end circuitry according to claim 5, wherein the impedance matching network comprises a plurality of differential L-networks.
12. (previously presented) The front-end circuitry according to claim 11, wherein the signal processing circuitry comprises a single-ended output.
13. (previously presented) The front-end circuitry according to claim 11, wherein the signal processing circuitry comprises a differential output.
14. (previously presented) The front-end circuitry according to claim 5, wherein the impedance matching network comprises a differential  $\Pi$ -network.
15. (previously presented) The front-end circuitry according to claim 14, wherein the signal processing circuitry comprises a single-ended output.
16. (previously presented) The front-end circuitry according to claim 14, wherein the signal processing circuitry comprises a differential output.

17. (previously presented) The front-end circuitry according to claim 14, wherein the differential  $\Pi$ -network comprises two inductors and two capacitors.
18. (previously presented) The front-end circuitry according to claim 5, wherein the impedance matching network comprises a plurality of differential  $\Pi$ -networks.
19. (previously presented) The front-end circuitry according to claim 18, wherein the signal processing circuitry comprises a single-ended output.
20. (previously presented) The front-end circuitry according to claim 18, wherein the signal processing circuitry comprises a differential output.
21. (previously presented) The front-end circuitry according to claim 5, wherein the impedance matching network comprises a differential T-network.
22. (previously presented) The front-end circuitry according to claim 21, wherein the signal processing circuitry comprises a single-ended output.
23. (previously presented) The front-end circuitry according to claim 21, wherein the signal processing circuitry comprises a differential output.
24. (previously presented) The front-end circuitry according to claim 21, wherein the differential T-network comprises four inductors and one capacitor.
25. (previously presented) The front-end circuitry according to claim 21, wherein the differential T-network comprises four capacitors and one inductor.
26. (previously presented) The front-end circuitry according to claim 5, wherein the impedance matching network comprises a plurality of differential T-networks.

27. (previously presented) The front-end circuitry according to claim 26, wherein the signal processing circuitry comprises a single-ended output.
28. (previously presented) The front-end circuitry according to claim 26, wherein the signal processing circuitry comprises a differential output.
29. (previously presented) The front-end circuitry according to claim 5, wherein the impedance matching network comprises at least one of a differential L-network, a differential  $\Pi$ -network, a differential T-network, or a combination thereof coupled in cascade.
30. (previously presented) The front-end circuitry according to claim 29, wherein the signal processing circuitry comprises a single-ended output.
31. (previously presented) The front-end circuitry according to claim 29, wherein the signal processing circuitry comprises a differential output.
32. (previously presented) The front-end circuitry according to claim 5, wherein the impedance matching network comprises a differential transmission line.
33. (previously presented) The front-end circuitry according to claim 32, wherein the signal processing circuitry comprises a single-ended output.
34. (previously presented) The front-end circuitry according to claim 32, wherein the signal processing circuitry comprises a differential output.
35. (currently amended) A radio-frequency (RF) apparatus, comprising:  
an impedance matching network, having a differential input having symmetrical impedances from input signal lines to a reference node, and a differential output having symmetrical impedances from output signal lines to the reference node; and

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a filter configured to receive a radio-frequency input signal, the filter having a differential output configured to provide a filtered radio-frequency (RF) signal to the impedance matching network.

36. (previously presented) The radio-frequency apparatus of claim 35, further comprising a signal-processing circuit having a differential input, the signal-processing circuit configured to accept a signal from the differential output of the impedance matching network.

37. (previously presented) The radio-frequency apparatus of claim 36, wherein the impedance matching network matches an output impedance of the filter to an input impedance of the signal-processing circuit.

38. (previously presented) The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises at least one differential L-network.

39. (previously presented) The radio-frequency apparatus of claim 38, wherein the signal-processing circuit comprises a low-noise amplifier.

40. (previously presented) The radio-frequency apparatus of claim 39, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.

41. (previously presented) The radio-frequency apparatus of claim 40, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

42. (previously presented) The radio-frequency apparatus of claim 41, further comprising a second integrated circuit comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

43. (previously presented) The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises at least one differential  $\Pi$ -network.



44. (previously presented) The radio-frequency apparatus of claim 43, wherein the signal-processing circuit comprises a low-noise amplifier.

45. (previously presented) The radio-frequency apparatus of claim 44, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.

46. (previously presented) The radio-frequency apparatus of claim 45, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

47. (previously presented) The radio-frequency apparatus of claim 46, further comprising a second integrated circuit comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

48. (previously presented) The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises at least one differential T-network.

49. (previously presented) The radio-frequency apparatus of claim 48, wherein the signal-processing circuit comprises a low-noise amplifier.

50. (previously presented) The radio-frequency apparatus of claim 49, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.

51. (previously presented) The radio-frequency apparatus of claim 50, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

52. (previously presented) The radio-frequency apparatus of claim 51, further comprising a second integrated circuit comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

53. (previously presented) The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises a cascade coupling of at least one differential L-network, at least one differential  $\Pi$ -network, at least one differential T-network, or a combination thereof.
54. (previously presented) The radio-frequency apparatus of claim 53, wherein the signal-processing circuit comprises a low-noise amplifier.
55. (previously presented) The radio-frequency apparatus of claim 54, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.
56. (previously presented) The radio-frequency apparatus of claim 55, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.
57. (previously presented) The radio-frequency apparatus of claim 56, further comprising a second integrated circuit comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.
58. (previously presented) The radio-frequency apparatus of claim 37, wherein the impedance matching network comprises a differential transmission line.
59. (previously presented) The radio-frequency apparatus of claim 58, wherein the signal-processing circuit comprises a low-noise amplifier.
60. (previously presented) The radio-frequency apparatus of claim 59, further comprising a first integrated circuit, wherein the low-noise amplifier resides within the first integrated circuit.
61. (previously presented) The radio-frequency apparatus of claim 60, wherein the first integrated circuit further comprises radio-frequency receiver circuitry.

62. (previously presented) The radio-frequency apparatus of claim 61, further comprising a second integrated comprising digital signal-processing circuitry, the second integrated circuit coupled to the first integrated circuit and configured to accept a digital output signal of the first integrated circuit.

63. (currently amended) A method of processing signals in a radio-frequency (RF) apparatus, comprising:

filtering an input radio-frequency signal in a filter that has a differential output configured to provide a filtered radio-frequency (RF) signal; and

receiving and processing the filtered signal in an impedance matching network that has a differential input having symmetrical impedances from input signal lines to a reference node, the impedance matching network configured to generate an output signal at a differential output of the impedance matching network, the differential output having symmetrical impedances from output signal lines to the reference node.

64. (previously presented) The method of claim 63, wherein the impedance matching network is configured to match an output impedance of the filter to an input impedance of the signal-processing circuit.

65. (previously presented) The method of claim 64, further comprising processing the output signal in a radio-frequency receiver circuitry.

66. (previously presented) The method of claim 65, wherein processing the output signal in a radio-frequency receiver circuitry comprises processing the output signal in a low-noise amplifier.

67. (previously presented) The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises at least one differential L-network.

68. (previously presented) The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises at least one differential  $\Pi$ -network.

69. (previously presented) The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises at least one differential T-network.

70. (previously presented) The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises a cascade coupling of at least one differential L-network, at least one differential  $\Pi$ -network, at least one differential T-network, or a combination thereof.

71. (previously presented) The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises a differential transmission line.

72. (previously presented) The method of claim 66, wherein the impedance matching network for receiving and processing the filtered signal comprises at least one of a differential L-network, a differential P-network, and a differential T-network.

73. (previously presented) The method of claim 72, wherein the low-noise amplifier for processing the output signal resides in a first integrated circuit that includes the radio-frequency receiver circuitry.

74. (previously presented) The method of claim 73, further comprising:  
receiving in a second integrated circuit a digital output signal of the radio-frequency receiver circuitry; and  
processing digitally the digital output signal of the radio-frequency receiver circuitry.

### **REMARKS AND INTERVIEW SUMMARY**

The Applicant thanks the Examiner for the Interview and discussion of the application. The Applicant received a telephone call from the Examiner to discuss the application and a possible amendment. During the Interview, the Applicant and the Examiner discussed claims 1, 35, and 63. The Examiner stated that he had reviewed the Applicant's remarks in the Response to Office Action dated September 22, 2005 ("Response"). The Examiner suggested amending claims 1, 35, and 63 to reflect the points the Applicant made in the Response regarding properties of differential networks. *See, e.g.,* Response at 4.

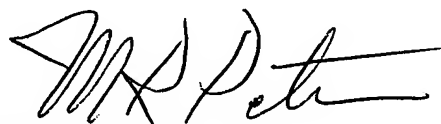
In response, the Applicant amends claims 1, 17, and 63. The Applicant makes the amendments to more particularly point out and distinctly claim a feature of the invention, rather than for reasons related to patentability or because of the cited references. The Applicant respectfully submits that the claims are in condition for allowance and requests a prompt Notice of Allowance.

### CONCLUSION

In view of the remarks above, the Applicant respectfully submits that the claims are in allowable condition. Consequently, favorable reconsideration and prompt issuance of a Notice of Allowance is respectfully requested. No fee is believed to be due. Should any fees under 37 CFR 1.16-1.21 be required for any reason relating to this paper, however, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/SILA:107.

The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'MR Peterson', written over a horizontal line.

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